Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**.38”**

**.044”**

**2 1 14 13 12**

**3**

**4**

**5 6 7 8 9**

**11**

**10**

**MASK**

**REF**

**Z008Y**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: Z008Y**

**APPROVED BY: DK DIE SIZE .038” X .044” DATE: 4/26/18**

**MFG: FAIRCHILD/NSC THICKNESS .015” P/N: 54AC32**

**DG 10.1.2**

#### Rev B, 7/1